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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/630,883	08/02/2000	Khosrow Golshan	82259/156	7954

7590 10/15/2004

EXAMINER	
CHANG, AUDREY Y	

ART UNIT	PAPER NUMBER
2872	

DATE MAILED: 10/15/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/630,883	GOLSHAN, KHOSROW	
	Examiner	Art Unit	
	Audrey Y. Chang	2872	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-78* is/are pending in the application.

4a) Of the above claim(s) *22-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-78* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remark

- This Office Action is in response to applicant's amendment filed August 4, 2004, which has been entered into the file.
- By this amendment, the applicant has amended claims 47, 65, 69, 73, and 77.
- Claims 23-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.
- Claims 47-78 remain pending in this application.

Drawings

1. The drawings were received on July 14, 2004. These drawings referring to Figure 9 are approved.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "720" and "705" have both been used to designate the same element in Figure 8. And the numerical references "730" and "710" designate the same part in Figure 8. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. Applicant's amendment **still fails** to correct the drawings for Figure 8.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 47-78 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification and the claims fail to teach what is considered to be an "*interference line*". It is known that when two coherent light beams intercept with each other, they interfere with each other. The wavefront of the coherent light beams are generally spread out and the wavefronts for the coherent light beams will intercept at **many different** locations and different directions, (please see the wavefront demonstration in Figures 2-5 in particular in this application), and since an interference region is claimed for the coherent light beams to intercept, it is therefore not possible to have just ***an*** interference line and event to determine ***an*** interference line.

5. Claims 68, 73 and 77 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification and the claims fail to teach how could "the interference region is configured to cause substantially no light exiting the interference region output when both *light and no light* is provided to both of first and second coherent light inputs", as recited in **amended** claim 73. It is not clear how could this be possible that no light exit from the interference region when light either enters or not enters the first and second optical paths. In particular, the claims are drawn to an optical logic circuit wherein *interference* between the light entering the interference region is *essential* requirement for the operation of the optical logic.

The specification and the claims also fail to teach how could the optical logic circuit provides **both the NOT and NOT AND** logical functions, as recited in claims 68 and 77. The applicant is

respectfully noted that page 6 of specification only discloses that the NOT AND (NAND) gate is used to **construct** a NOT gate. The specification does not give positive support for the logic function to be **BOTH** the NOT and NOT AND gates.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 47-58, and 63-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Usagawa et al (PN. 5,233,205).

Usagawa et al teaches an *optical logic circuit* based on quantum well design wherein the optical logic circuit comprises a *substrate* comprising a *first optical material*, (such as 50 in Figure 5A or 95 in Figure 6A or 6B), and *a second optical layer overlaying the substrate* wherein the second optical layer are formed or patterned to have a plurality of *optical pathways* or *optical conduits*, (52 in Figure 5A or 100, 101 and 102 in Figure 6B), wherein an *interference regions* are formed of the second optical layer as shown in Figures 1A to 1G. Usagawa et al teaches that a plurality of *waveguides* (3, 4, and 5) are used to provide *optical input signals* to a plurality of *input gates* (10, 10' and 10"), wherein the optical input signals enter a three-dimensional region surrounded by potential barrier (1), which then serves as the *interference region*, that includes or is connected to at least one *output window* (300') such that the input optical signals intercept and interfere with each other. An *output gate* (20, Figures 1A to 1G) is connected with the interference region to provide an *optical output signal.* Usagawa et al teaches that the optical output signal is a *Boolean logic output signal*, wherein the optical logic circuit can be designed to

provide NOT (invert, Figure 1D), NOT AND (NAND, Figure 1F), and exclusive OR (NOR Figure 1G) optical logic functions, respectively.

With regard to claims 48, 51, 56-58, 66, 70-72, and 74, Usagawa et al teaches the optical logic circuit may be designed to give NOT logic function as the output signal, (Figure 1D), wherein an optical input signal may be a *constant coherent input signal*, ("1") that enters the interference regions through the input gate (10), and a *second input coherent optical signal* (X) may be switched ON or OFF and enters the interference region through the *second input gate* (10'). When the second coherent input signal is turned ON, the input signals from both gates interfere with each other to essentially cancel each other so that an invert or NOT optical logical function is resulted as the optical output signal, (please see Figure 1D, column 8, lines 8-25).

With regard to claims 49-50, 67, 68, 69, 75, and 77, Usagawa et al teaches that the optical logic circuit may be designed to give NAND logic function, (Figure 1F), wherein three input optical signals are used.

This reference has met all the limitations of the claims with the exception that an interference line is aligned with the output. However it is not clear what is considered to be the interference line for the reasons stated in the rejection above. But it is understandable that the output gate must be arranged so that the resultant output signal, after the interference as the result of the interference, can be propagated out of the interference region. Such feature is therefore either inherently met or an obvious modification to one skilled in the art to make the optical logic gate more efficient.

With regard to claims 63 and 64, this reference also does not teach explicitly that a laser diode or a semiconductor diode is used as the light source for generating the optical wave. However laser diode or laser semi-conductive diode are both well known light sources for operating optical logic circuit, such feature is either inherently met or an obvious modification to one skilled in the art for providing proper light sources with proper energy required to operate the optical logic circuit.

Claim 47 has been amended to include the feature of the "interference line is aligned with the output when the light input at the second input is on". This feature is implicitly included in the disclosure since only when light propagates through the pathways, the quantum waves are generated.

8. **Claims 59-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Usagawa et al as applied to claim 55 above, and further in view of the patent issued to Logan et al (PN. 3,837,728).**

The optical logic circuit taught by **Usagawa** et al as described for claim 55 above has met all the limitations of the claims. Usagawa et al teaches that the optical logic circuit may use gallium arsenide (GaAs) material as the substrate layer however it does not teach explicitly to use doped GaAs material, silicon or doped silicon materials as the substrate layer and optical layer for pathways (i.e. waveguides) respectively. However these materials are all well known semi-conductive materials for making waveguides or even optical logic circuit, as demonstrated by the teachings of Logan et al wherein a GaAs layer is used as substrate layer wherein doped GaAs layer is used as the optical waveguide. It would then have been obvious matters of design choices to one skilled in the art to use the claimed materials as the materials for designing the optical logic circuits for the benefit of using desired materials that provide the desired performance. It has also been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended used as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Response to Arguments

9. Applicant's arguments filed on July 14, 2004 have been fully considered but they are not persuasive.

10. Applicant fails to provide the arguments concerning the rejection of "interference line". The applicant is respectfully requested to indicate in which response paper did the applicant has responded to this issue if such has already been addressed before.

11. Applicant's arguments concerning the rejections of claims 68, 73 and 77 have been fully addressed in the paragraphs above.

12. In response to applicant's arguments, which state that the cited Usagawa reference teaches a logic circuit based on *quantum well structure*, which therefore is not an optical logic circuit that based on light sensitive material and device, the examiner respectfully disagrees for the reasons stated below. Firstly, the both the cited reference and the instant application used *semi-conductive material*, (please see page 9 of the instant application) for designing the logic circuit. This means that the material used to design the logic circuit of Usagawa reference is *as optical sensitive* as the material used in the instant application. Secondly, it is known in the art that the quantum wave behavior of the electron and hole carriers are *induced* by incident light propagates through the material, (the applicant is respectfully noted that electrons and holes in a semi-conductor material do not have enough energy on their own to propagate through the medium unless an excitation light is incident to excite the electrons to the conduction energy band, please see Figure 10 of Suzuki (PN. 5,754,714)). Thirdly, Usagawa reference teaches that "electron waves" are entering the interference regions to produce interference effect, (i.e. wavelike behavior), where it is known in the art that an electron wave is an electromagnetic wave just as a "light wave" is an electromagnetic wave". This reference therefore reads on the claims.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Audrey Y. Chang whose telephone number is 571-272-2309. The examiner can normally be reached on Monday-Friday (8:00-4:30), alternative Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Dunn can be reached on 571-272-2312. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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